METHOD AND APPARATUS FOR NESTED CONTROL FLOW

ABSTRACT

A method and apparatus for nested control flow includes a processor having at least one context bit. The processor includes a plurality of arithmetic logic units for performing single instruction multiple data (SIMD) operations. The method and apparatus further includes a first memory device storing a plurality of instructions wherein each of the plurality of instructions includes a plurality of extra bits. The processor is operative to execute the instructions based on the extra bits and in conjunction with a context bit. The method and apparatus further includes a second memory device, such as a general purpose register operably coupled to the processor, the second memory device receiving an incrementing counter instruction upon the execution of one of the plurality of instructions. As such, the method and apparatus allows for nested control flow through a single context bit in conjunction with instructions having a plurality of extra bits.